DUAL DENSITY 5 1/4" FLOPPY DISK CONTROLLER BOARD

PRODUCT SPECIFICATION

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1.0 SCOPE

This specification covers the functional, electrical, mechanical, environmental, quality, and reliability requirements for a Double Density Disk Controller.

1.1 INTRODUCTION

This document describes the organization and operation of a dual density disk controller board which can be used with the 99/4X Peripheral Expansion Chassis. The board will interface one to four 5 1/4 inch floppy disk drives of single or double data density, one or two heads, 35/40 (48 TPI) or 77 (96 TPI) tracks per side.*

The controller hardware is designed around an NEC uPD765 disk controller chip (Intel 8272 second source). The board is downward compatible with the existing 99/4 single density controller on a functional basis; i.e., any diskette written with the old single density controller can be read by this controller on a 48 TPI or 96 TPI drive and any single density, 48 TPI diskette written with this controller can be read by an old controller.

2.0 APPLICABLE DOCUMENTS

1. TI 99/4 Disk Peripheral Software Specification version 1.0 dated 2/25/80.
2. Functional Specification for the 99/4 Disk Peripheral version 2.0 dated 10/22/79.
3. 99/4 Disk Peripheral GPL Interface Specifications version 1.0 dated 2/20/80.
4. Approaches to a Double Density Disk Controller Design for the 99/4X dated 1/11/82.
5. NEC uPD765 Single/Double Density Floppy Disk Controller Data Sheet dated 10/80.
6. ANSI Standard X3.80-1981 Interfaces Between Flexible Disk Cartridge Drives and Their Host Controllers.
7. Functional Requirements for a Dual Density 5 1/4" Floppy Disk Controller Board dated 2/8/82.
8. Data Sheet for FDC9216 Floppy Disk Data Separation from Standard Microsystems Corporation dated 1981.

3.0 SPECIFICATIONS

The 99/4X dual density disk controller hardware and device service routine (DSR) software will format, read, and write diskettes of the following configurations:

* (TPI = Tracks Per Inch)

No. Trks.	No. Sides	Data Density	Sectors/ Track	Sectors/ Diskette	Data Bytes/ Diskette
35	1	S	9	315	80640
35	1	D	16	560	143360
40	1	S	9	360	92160
40	1	D	16	640	163840
40	2	S	9	720	184320
40	2	D	16	1280	327680
77	1	S	9	693	177408
77	1	D	16	1232	315392
77	2	S	9	1386	354816
77	2	D	16	2464	630784

All sectors are 256 data bytes long. Single data density follows IBM 3740 FM encoding format and double density is IBM 34 MFM format.

Jumpers on the board must be jumped to indicate presence of a 77 (96 TPI) drive, or else, the default (no jumper) selection is 35/40 (48 TPI). Jumpers may also be installed for each drive to indicate other than the standard 20 millisecond head step rate. Additional step rates are 32, 12, and 6 milliseconds.

Data density is automatically determined by the low level DSR in the read or write mode. If the 77 track jumper is installed, the DSR will also automatically adjust to read or write a 48 or 96 Track Per Inch formatted diskette.

4.0 HARDWARE ORGANIZATION

4.1 GENERAL

The dual density disk controller hardware is contained on a standard peripheral expansion box printed circuit board measuring approximately 5 X 7 inches. A 34 pin connector conforming to ANSI Standard X3.80-1981 for 5 1/4 inch disk drive interconnection is mounted to the rear of the board and protrudes from the expansion box. As illustrated on the System Block Diagram of Appendix A, the controller board interfaces to the system CPU thru the 60 pin expansion box bus. All signals to or from this bus are buffered on the board.

4.2 MEMORY ALLOCATION

In keeping with 99/4 peripheral concepts, the controller board contains the DSR ROM necessary to run the disk functions. This ROM is located in the common DSR CPU space of >4000 to >5FFF and is selected by CRU bits unique to the disk controller. Portions of the ROM space are decoded to control the 765 disk controller chip. The CRU address block resides between >1100 and >11FE, which is the same as the present single density controller (no two disk controller boards can be simultaneously plugged into the peripheral box).

The CRU memory bank select bit expands the DSR space from the standard 8 kbytes to 12 kbytes. The 128 byte RAM provides space for saving portions of the 16 bit wide CPU workspace RAM (the DSR byte-move loop must be located is fast RAM to keep up with double density transfer rates) and also provides additional workspace for the new DSR.

Memory assignment is as follows:

>4000-4EFF	ROM A	3840	bytes from a TMS4732(4K x 8)
>4F00-4F7F	RAM	128	bytes from a MCM6810(128 x 8)
>4F80-4FEF	unused	112	bytes
>4FF0-4FFF	765	16	bytes for controller chip commands
>5000-5FFF	ROM B1	4096	bytes from 1/2 TMS4764(8K x 8)
>5000-5FFF	ROM B2	4096	bytes from 1/2 TMS4764

ROM B is bank selected by a CRU latch similar to the method used on the P-Code peripheral board. This bit (HIHALF) provides the MSB of address for the 8K byte ROM.

4.3 CRU ASSIGNMENTS

CRU bits are assigned as follows (all are active high):

OUTPUTS

>1100	DSRBIT	Enables DSR Memory space >4000-5FFF
>1102	MOTBIT	Triggers 5 second 1-shot for drive motors on
>1104	WAIBIT	Enables wait logic for 765 control of CPU READY
>1106	HIHALF	Memory bank select for upper half of 8K ROM
>1108	DACK	Data Acknowledge to satisfy 765 after Scan cmd.
>110A	LED	Turns on LED indicator
>110C	MOTSTR	Triggers Motor Start 850 msec 1-shot
>110E	FDRST	Reset to 765 FDC chip
>1110	DSEL1	Selects Drive no. 1
>1112	DSEL2	Selects Drive no. 2
>1114	DSEL3	Selects Drive no. 3
>1116	DSEL4	Selects Drive no. 4
>1118	PREDIR	Sets Direction signal to move head inward
>111A	PRESTP	Raises Step signal to move head 1 step
>111C	NOCOMP	Disables write precompensation circuit
>111E	unused	

INPUTS

>1100	FDINT	Interrupt signal from 765 FDC chip
>1102	DVENA	Drive enable signal from 5 second 1-shot
>1104	MOTSPD	Motor up to speed signal from 850 msec 1-shot
>1106	HIHALF	Memory bank select signal from CRU output
>1108	DR1TK	Drive no. 1 track jumper (1=no jumper=48 TPI)
>110A	DR1ST0	Drive no. 1 step jumper #0
>110C	DR1ST1	Drive no. 1 step jumper #1

>110E	DR2TK	Drive no. 2 track jumper
>1110	DR2ST0	Drive no. 2 step jumper #0
>1112	DR2ST1	Drive no. 2 step jumper #1
>1114	DR3TK	Drive no. 3 track jumper
>1116	DR3ST0	Drive no. 3 step jumper #0
>1118	DR3ST1	Drive no. 3 step jumper #1
>111A	DR4TK	Drive no. 4 track jumper
>111C	DR4ST0	Drive no. 4 step jumper #0
>111E	DR4ST1	Drive no. 4 step jumper #1

The above step jumpers select step rates for each drive as follows (shown are actual CRU input logic levels where 1=no jumper installed):

Jumper #1	Jumper #0	Step Rate (msec)
1	1	20
1	0	32
0	1	12
0	0	6

4.4 CLOCKS

The 8 MHZ crystal controlled clock generator is divided down to provide the following frequencies appropriate to single or double density:

	S.D.	D.D.
765 clock	4 MHz	4 MHz
765 write clock	250 KHz	500 KHz
Data separator	4 MHz	4 MHz
Write precomp.	8 MHz	8 MHz

The 765 write clock frequency is controlled by the MFM output signal from the 765 FDC chip. This is a nonsymetrical clock with a 250 nsec active high time per the 765 spec.

4.5 ADDRESS DECODE LOGIC

Address lines are buffered thru 74LS244 buffers and are decoded by two field programmable logic arrays (PAL's) and TTL logic. The PAL's are 12L6's (used on prior peripheral boards) with 12 inputs and 6 outputs. Logic equations for the PAL's are as follows:

PAL A

PIN1=/(PCBEN*AMC.B*AMB.B*AMA.B) (decoded by external 74LS20)

/CRUENL=(/PIN1*/MEMEN*/A00.B*/A01.B*/A02.B*A03.B*/A04.B*/A05.B*/A06.B*A07.B*/A11.B) + (PIN1*/PIN1) + (PIN1*/PIN1) + (PIN1*/PIN1)
where (PIN1*/PIN1) merely fillout remaining OR terms with 0.

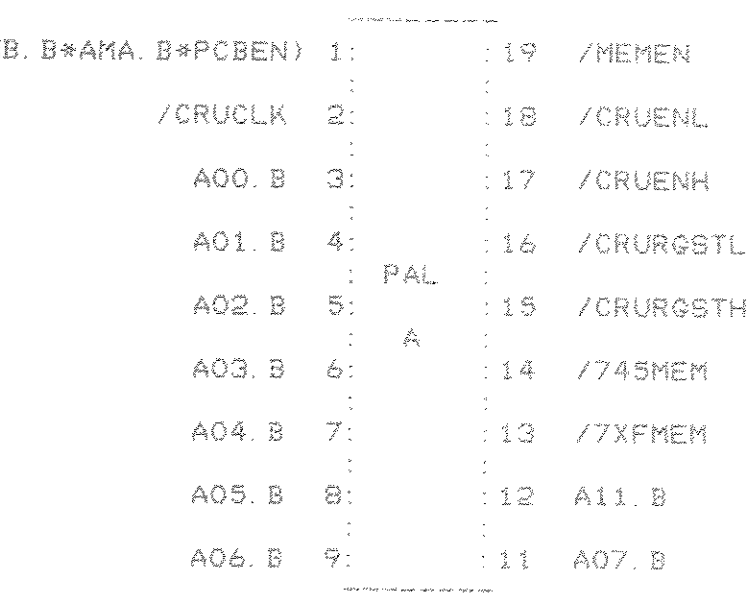
/CRUENH=(/PIN1*/MEMEN*/A00.B*/A01.B*/A02.B*A03.B*/A04.B*/A05.B*/A06.B*A07.B*A11.B) + (PIN1*/PIN1)

/CRURGSTL=(same as /CRUENL) * (CRUCLK) + (PIN1*/PIN1)

/CRURGSTH=(same as /CRUENH) * (CRUCLK) + (PIN1*/PIN1)

/745MEM=(/PIN1*MEMEN*/A00.B*A01.B*/A02.B) + (PIN1*/PIN1)

/7XFMEM=(/PIN1*MEMEN*A04.B*A05.B*A06.B*A07.B) + (PIN1*/PIN1) +
(PIN1*/PIN1) + (PIN1*/PIN1)



PAL B

/FDSEL=(745MEM*7XFMEM*A08.B*A09.B*A10.B*A11.B*/A03.B*DSRBIT) +
GND + GND +GND
where GND provides logic 0 input to remaining OR terms

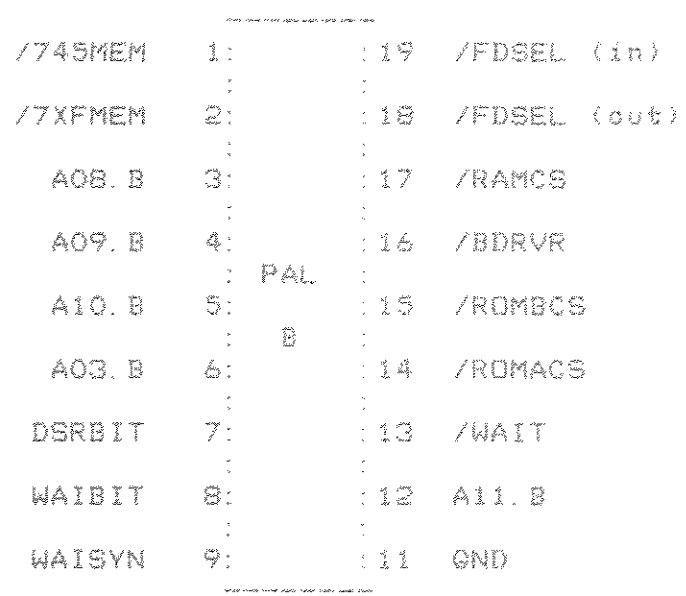
/RAMCS=(7XFMEM*745MEM*/A08.B*/A03.B*DSRBIT) + GND

/BDRVR=(745MEM*DSRBIT) + GND

/ROMBCS=(745MEM*A03.B*DSRBIT) + GND

/ROMACS=(745MEM*/7XFMEM*/A03.B*DSRBIT) + GND

/WAIT=(FDSEL*WAIBIT*WAISYN) + GND + GND +GND



4.6 WAIT LOGIC

The Wait logic produces a not ready condition for the CPU on memory cycles which require the 765 chip to perform some prolonged task. The CPU Ready line goes active at the end of the task, thus causing the 765 to appear as very slow memory. The wait logic is enabled by CRU bit 1104 (WAIBIT). Immediately upon selection of the 765 chip (FDSEL), READY.A is brought low by /WAIT from PAL B. /WAIT and READY.A stay low until a Data Request (DRQ) signal is raised by the 765 chip. DRQ indicates that the 765 is ready to send or receive a byte over the data bus. DRQ clears Wait Sync.(WAISYN) via the 74LS74 flipflops which causes /WAIT to go inactive and releases READY.A. The CPU then delivers or takes in the byte by issuing a Read or Write Data command to the 765. Either of these commands also forces Data Acknowledge (/DACK) low to the 765 and releases DRQ which in turn raises WAISYN and starts another not ready cycle. This continues until all 256 bytes of data have been transferred at which time DRQ stays low. WAISYN is also cleared under abnormal conditions by the 765 interrupt (765 is unable to locate the sector) or the motor speed (MOTSPD) timer running out (765 FDC locks up due to no diskette or trying to read single density data in double density mode).

The Wait logic is enabled only when actually reading or writing a sector where data bytes must be transferred between CPU and 765 FDC.

4.7 CONTROLLER CHIP

The NEC uPD765 Floppy Disk Controller chip (2nd sourced by Intel 8272) was selected because it provides on-board read-after-write compare. This function cannot be done by software alone at double density transfer speeds. Additionally, the 765 provides internal generation of data and gap fields while formatting. Other features such as simultaneous head positioning are not presently utilized.

The CPU communicates with the 765 FDC via memory mapped addresses as follows:

>4FF0 Read 765 Main Status Register
>4FF2 Read a Data byte from 765 Data Register
>4FF4 Read a Result byte from 765 Data Register
>4FF8 Write a Command byte to 765 Data Register
>4FFA Write a Data byte to 765 Data Register

>4FFE Wait for DRQ from 765 (DRQWAT) - enables Wait logic

Detail operation of the 765 chip is discussed in the 765 data sheet (Applicable Document 5).

4.8 DRIVE SELECTION AND HEAD POSITIONING

Drives are independently selected by CRU bits 1110,2,4,6 which activate signals DSEL1,2,3, or 4 provided the 5 second timer has turned all drive motors on and enabled the drive select buffers (74LS38) with DVENA. CRU drive select was implemented, rather than using the 765 select signals, in order to stay common with the previous controller operation and allow for longer drive select times. The 765 head load signal (HDL) is also not used since all drives are internally wired to load their heads when the drive is selected. Side selection is controlled by the 765 signal HD which is sent to the drive as /SIDSEL. The 765 raises HD in response to a Read or Write data command which specifies Side 1.

Head positioning is normally controlled by FR/STP step signal and LCT/DIR direction signal from the 765. The 765 activates these signals when it receives a SEEK command which specifies a new track different from what the 765 has stored in its internal Present Cylinder Number (PCN) register. The 765 calculates direction and number of steps required to reach the new track and issues the appropriate signals. Its PCN register is then updated with the new track number. The PCN cannot be loaded from the CPU, but can be zeroed by issuing a RECALIBRATE (Restore) command.

Under the unusual circumstance when a 77 track (96 TPI) drive must read a 35 or 40 track (48 TPI) diskette, the DSR must pre-step the head one half the required steps to the new track position and then issue a 765 SEEK command for the remaining steps. This pre-stepping is done at a fixed 32 msec. step rate via CRU bit 110A (PRESTP) with direction set by bit 1108 (PREDIR). These signals are wired-or'd to the normal /STEP and /DIR drive signals. The 77 track drive jumper must be installed to enable this feature.

4.9 DATA SEPARATION

Separation of composite read data and clock from the drive is accomplished with the single chip FDC9216 Floppy Disk Data Separator chip from Standard Microsystems Corporation (applicable document no. 8). This 8-pin chip uses the 4MHz clock for reference and the 765

MFM output to designate single or double density (MFM high) mode. The 9216 provides Read Data (RDD) and Read Data Window (RDW) to the 765.

4.10 WRITE PRECOMPENSATION

Most drive manufacturers recommend write precompensation for double data density writing. This adjusts actual bit write-time depending upon the clock/data pattern being written. Time skew on read due to closely packed flux transitions is thus compensated.

The write precompensation circuit on the controller board (74LS164 and 74LS251) is enabled for all write operations and is controlled by Precompensation outputs PS0 and PS1 from the 765. Driven by the 8MHz clock, the LS164 adjusts the 765 Write Data (WDA) +/- 125 nsec. to form Early, Normal, or Late clock/data (/WTDATA) for the drive. The write precomp. can be disabled by CRU bit 111C (NOCOMP) if later needs dictate.

4.11 ELECTRICAL CONNECTIONS

Electrical connections to the 60 pin peripheral box bus are as follows:

PIN	SIGNAL	DIRECTION CPU	DIRECTION Controller
1,2	+5v unregulated		>
3,5,7	Ground		~
20,27	"		~
47,49	"		~
53	"		~
4	READY.A	<	>
6	/RESET	>	>
8	N/C		
9	N/C		
10	N/C		
11	/RDBENA	<	
12	PCBENA	>	
13	N/C		
14	N/C		
15	N/C		
16	/SENILB	<	
17	N/C		
18	/INTB		<
19	D7	<>	<>
21	D5	<>	<>
22	D6	<>	<>
23	D3	<>	<>
24	D4	<>	<>
25	D1	<>	<>
26	D2	<>	<>
28	D0	<>	<>
29	A14.A	>	

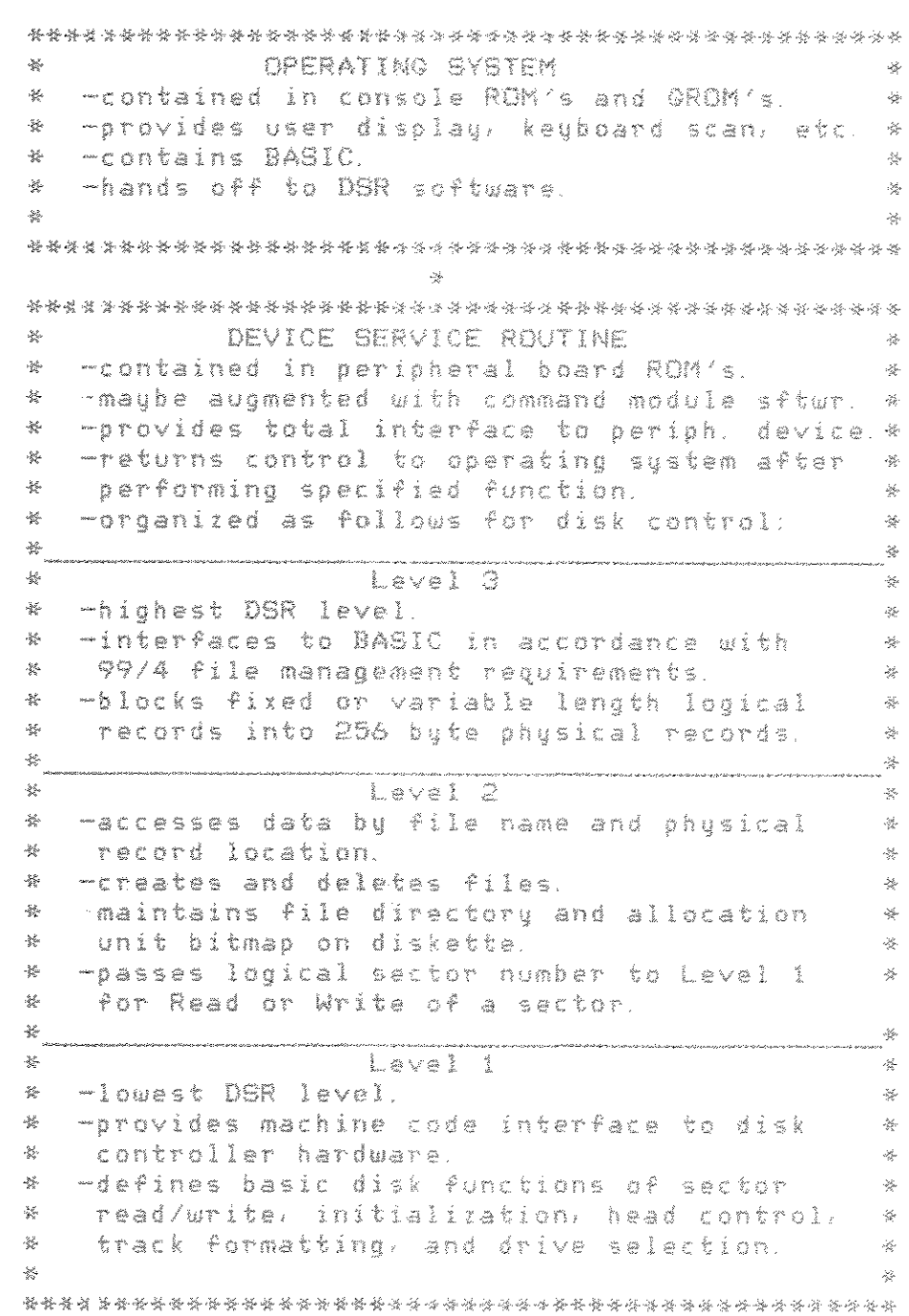
30	A15/COUT.A	>
31	A12.A	>
32	A13.A	>
33	A10.A	>
34	A11.A	>
35	A08.A	>
36	A09.A	>
37	A06.A	>
38	A07.A	>
39	A04.A	>
40	A05.A	>
41	A02.A	>
42	A03.A	>
43	A00.A	>
44	A01.A	>
45	AMB.A	>
46	AMA.A	>
48	AMC.A	>
50	/CLKOUT.A	>
51	/CRUCLK.A	>
52	DBIN.A	>
54	/WE.A	>
55	CRUIN	<
56	/MEMEN.A	>
57	N/C	
58	N/C	
59	N/C	
60	N/C	

Signals to the 34 pin disk drive connector are in accordance to ANSI Standard X3.80-1981 and are as follows:

PIN	SIGNAL	DIRECTION Controller	DIRECTION Drive
2	Not Assigned		
4	Not Assigned		
6	Drive Select 3	>	
8	Index	<	
10	Drive Select 0	>	
12	Drive Select 1	>	
14	Drive Select 2	>	
16	Motor ON	>	
18	Direction Select	>	
20	Step	>	
22	Composite Write Data	>	
24	Write Gate	>	
26	Track 0	<	
28	Write Protected	<	
30	Composite Read Data	<	
32	Side One Select	>	
34	Not Assigned		
1-33	Ground - all odd number pins		

5.0 SOFTWARE ORGANIZATION

Overall software structure may be viewed as follows:



Since Levels 2 and 3 of the DSR comprise approximately 6.5 kbyte of the 8 kbyte DSR ROM, substantial savings in software design can be achieved by preserving this software. DSR Level 1 software must be changed to accommodate double density features and the new 765 controller chip. The hardware design will not preclude future changes to Level 2 and 3 software (variable sector lengths, double density tracks, handling of 4 drives, etc.).

Additional disk related software resides in the Disk Manager command

module to provide the following utility functions:

-Single disk backup
-Disk to disk copy/backup
-Disk initialization/formatting
-Disk catalog
-Disk rename
-Disk test
-File copy
-File rename
-File protection status
-Selective file deletion

Segmentation of the DSR into the bank selected 12kbyte available ROM is flexible. The software delivered with the prototype board has the high level DSR residing in >4000-5FFF (less RAM and 765 space) of the initial 8kbytes and the new low level DSR in the bank selected >5000-5FFF. Calls to the low level DSR are made thru 'DSKENT' which switches on the upper bank and turns it off on return.

6.0 OPERATION

6.1 GENERAL

To eliminate the need for user prompts or option select switches (with the exception of track density and step rate jumpers discussed in the CRU section), routine disk read/write operations will depend on pre-formatted diskette information to tell the DSR how to select controller options. Options will be determined as follows:

1. Single or Double Data Density - The controller will attempt to read a specified sector address ID at the start of a Read or Write sector operation. The controller may be in single or double data density mode.

   If no address can be read (765 'Missing Address Mark' error), the controller will shift to the alternate data density mode and attempt a read. The correct density mode will be stored in the 'Density' byte in onboard RAM for the particular drive and will remain valid until the next 'Missing Address Mark' error (usually diskette change or board power-up).

2. Single or Double Side - The low level DSR calculates track and physical sector number from the logical sector number passed from the high level DSR. If the calculated track number exceeds the max. tracks available for the drive on Side 0 (determined by the 40/77 trk. jumper), the DSR extends the calculation to Side 1. The algorithm places the next excess sector on the inner track of Side 1 so that the head can sweep from outer (Track 00) to inner track of Side 0 then inner to outer track of Side 1. This technique coincides with the old controller DSR.

3. Single or Double Track Density - If the track density jumper of a drive has a jumper wire inserted, the drive is designated as a 96 Track Per Inch drive (see CRU section). No jumper inserted specifies a 48 TPI drive compatible with the old controller. In the 96 TPI mode, the controller will handle up to 77 tracks per side. Either 35 (single sided only) or 40 tracks can be accessed in the 48 TPI mode.

   If the 96 TPI jumper is installed, the DSR will force the controller to read a 48 TPI formatted diskette. (See section on Drive Selection and Head Positioning.) As a final error retry, the DSR restores the head to Track 00 then steps the head inward 2 steps. A Read ID command then reads the diskette track number. If the result is Track 01, the DSR switches to a Drive Different mode and indicates the 77 track drive is accessing a 35/40 track diskette by setting a flag in the drive's DRVDIF byte. This mode is retained until a new error retry is forced (diskette change or board power-up).

4. Variable Step Rate - As described in the CRU Section, jumpers are available on the board to designate step rates of 20 milliseconds (default rate with no jumpers installed), 6, 12, or 32 milliseconds. The jumpers are scanned and the proper rate is sent to the 765 controller chip via the Specify command when the drive is first accessed.

5. Variable Sector Length - The present high level DSR supports only 256 bytes/sector and this fixed length is carried over into the new DSR. The 765 controller chip will support the 4 sector lengths provided for in IBM format (128, 256, 512, and 1024 bytes/sector).

Parameters are passed between high level DSR (Levels 2 and 3) and the low level DSR (Level 1) via the following CPU 256 byte RAM locations (referenced to starting address >8300 for the TMS9900):

SEC	>4A	Logical sector number (two bytes). In Format, used to return no. of sectors/disk.
DRIV	>4C	Drive number (1-4 possible, 1-3 now used) byte. If the MSB of DRIV is a 1, then files are to be read from or written to CPU expansion RAM instead of VDP RAM.
RW	>4D	Read (nonzero) or Write to the disk. In Format, passes no. of tracks/side to low level DSR and returns no. of sectors/track.
MEMSTA	>4E	CPU or VDP RAM Start address.
STAT	>50	Status return from low to high level DSR. In Format, provides data density (0 or 1=SD, 2=DD) to low level DSR.
SIDES	>51	Used in Format only to provide no. of sides per diskette.
STORE	>58	Address of disk VDP block (not used).

6.2 FUNCTIONAL FLOW

Disk operation falls into the following categories when using the commands of the 765 disk controller chip in a way compatible with the existing DSR structure (see ref. 5):

1. Specify - Sets DMA mode; Step Rate Timer (2-32 msec @ 2 msec intervals); Head Load Timer (4-508 msec @ 4 msec intervals); and Head Unload Timer (32-480 msec @ 32 msec).

2. Recalibrate - Steps drive head outward until Track 0 signal is sensed or until 77 steps are taken (error condition).

3. Seek - Steps drive head the required number of steps in the direction necessary to reach the specified new track.

4. Read ID - Reads first ID field encountered on diskette and returns track number, side number, sector number, and number of bytes per sector for verification of head position.

5. Format Track - Writes complete track starting at index mark and formats track according to IBM standards for single or double density data. Bytes per sector and sectors per track are selectable.

7. Read Data - Reads specified sector.

8. Write Data - Writes specified sector.

9. Scan Equal - Performs read-after-write comparison on a specified sector on a byte basis except where a >FF mask byte is located in memory or on the disk.

10. Sense Interrupt Status - Reads 765 Status Register 0 to determine cause of 765 issued interrupt and clears interrupt.

With the above features available on the 765 controller chip, the fundamental disk operations appear as follows:

INITIALIZE - POWER UP ROUTINE
'INITAL' or 'INITL' when linked thru bank select routine

1. Sets Motor On, which starts a 5 second pulse to activate all drive motors.

2. Writes >FF to all drive track registers (TRK bytes) to indicate the need to Restore all drive heads to Track 00 on first access.

3. Sets all drive density mode bytes (DENSTY) to zero for

single density.

4. Resets 765 Floppy Disk Controller chip via CRU bit.

5. Clears miscellaneous flag bytes in onboard RAM.

6. Set status return CPU RAM location >50 "STAT" to >0100. This indicates to the high level DSR calling routine that no Seek/Step error has occurred.

7. Front panel LED is lighted during DSR activity.

READ OR WRITE A SECTOR
'SECIO' or 'SECL'

1. Turns on board LED.

2. Utilizes one or more of the following subroutines:

CALCULATE TRACK ('CALTRK') - CALCULATES PHYSICAL TRACK & SECTOR NO.

1. Sets up common command bytes for 765 FDC read or write command.

2. Divides passed logical sector number by number of sectors per track for present density mode to obtain physical track, sector, and side number.

3. If Drive Different flag (DRVDIF) is set, then number of Presteps is calculated and Predirection is set.

4. Branch is made to either Read or Write Sector depending on passed value of 'RW'.

SPECIFY ('SPECFY') - SPECIFIES DRIVE PARAMETERS FOR FDC CHIP

1. Checks "DRIV" for valid drive number and converts it to drive index 0-3 in "TEMP1" workspace register.

2. Sets up CPU speed index in "CPUINX" workspace register (0=TMS9900, 2=other to be defined later).

3. Turns drive motors on by triggering (or retriggering) 5 second hdwr. 1-shot (MOTBIT). If 1-shot is not already on, then an additional 850 msec. 1-shot (MOTSTR) is triggered to indicate motors are coming up to speed.

4. If drive no. is different from last drive accessed, then drive parameter jumpers are scanned and a 'Specify' command is sent to the 765 FDC containing the following:
   - Head Unload Time (HUT) fixed at a maximum 480 msec.

to avoid head load time penalties for closely spaced disk accesses. (CRU actually controls head load via drive select bits.)
- Head Load Time (HLT) set at 16 msec. to provide a settle time between head moves.
- DMA mode is set so FDC requests each R/W byte with a DRQ signal.
- Head Step Rate (SRT) is set at 20, 6, 12, or 32 msec. depending on drive jumper setting.

5. Also if drive no. is different from last drive accessed, the old drive select CRU bit is turned off and the new drive select is turned on. And a software timed-out delay of approximately 75 msec. allows for the new drive head to settle after CRU drive select.

RESTORE ('RESTOR') - MOVES HEAD TO TRACK 00

1. Sends 'Recalibrate' command to 765 for drive unit indicated by CPU RAM location >4C "DRIV". The DSR loops and waits for the 765 interrupt pin to indicate the head reached Track 00 or 77 steps were taken (error condition).

2. Sends 'Sense Interrupt Status' command to 765 to determine if Track 00 reached or error condition exists and to clear 'Recalibrate' interrupt.

3. If Track 00 reached, writes zero to selected drive track storage byte (TRK) in onboard RAM. Otherwise, returns "NODISK" error (00010110) in CPU RAM "STAT" byte >50, and sets no drive present flag (>A5) in TRK. With >A5 present in drive's TRK byte, the DSR will no longer try to access the particular drive, but will return an immediate "NODISK" error. Only a real board-power-down will overcome this condition.

FALSE STEP ('FALSTP') - PRESTEPS HEAD 1/2 DISTANCE IF 96 TPI DRIVE IS READING 48 TPI DISKETTE

1. Steps selected drive head no. of steps specified by workspace register VALUE in the direction already set by CRU bit PREDIR (see section on Drive Selection and Head Positioning).

2. Step rate is fixed by software timeout loop at 32 msec.

SEEK ('HDPOS') - MOVES SELECTED DRIVE HEAD TO NEW TRACK

1. Send 'Seek' command to 765 with new track designated by drive's 'TRK' track RAM location.

2. Controller chip will step head until new track is reached The software waits in a loop until the 765 indicates execution is completed by raising its interrupt signal.

3. Send 'Sense Interrupt Status' command to 765 to clear 'Seek' completion interrupt and check for error condition. This command also reads the updated Present Cylinder Number register of the 765 which is then compared with the intended new track number.

4. If 765 returns error condition, then initiate 'Seek Error' retry. If no interrupt is raised by 765 before 5 sec. 1-shot times out, then hard 'No Disk' error is sent to high level DSR.

SAVE CPU RAM ('SAVLOP') - SAVES SECTION OF 16-BIT CPU RAM INTO BOARD RAM SO BYTE TRANSFER LOOP CAN BE EXECUTED OUT OF FAST RAM

1. Moves 22 byte section of CPU RAM starting at location defined by workspace register 'CPU' into onboard RAM.

2. Sets 'SAVFLG' onboard RAM flag to prevent additional save operation before Return subroutine restores original code.

READ DATA ('RSEC') - READS ONE SECTOR FROM DRIVE

1. Read Byte Transfer Loop is moved into 16-bit CPU RAM starting at 'CPU' location (see above 'SAVLOP').

2. MSB of 'DRIV' is checked to determine if memory is VDP (=0) or CPU (=1) RAM and VDP address register is setup to read VRAM if necessary; otherwise, the byte transfer loop is set to autoincrement memory address.

3. Setup 'Read Data' cmd. for 765 and go to common Read/Write routine for execution.

WRITE DATA ('WSEC') - WRITES ONE SECTOR TO DISK

1. Write Byte Transfer Loop is moved into 16-bit CPU RAM starting at 'CPU' location (see above 'SAVLOP').

2. MSB of 'DRIV' is checked to determine if memory is VDP (=0) or CPU (=1) RAM and VDP address register is setup to write VRAM if necessary; otherwise, the byte transfer loop is set to autoincrement memory address.

3. Setup 'Write Data' command for 765 and go to common Read/Write routine for execution.

4. If no error conditions, proceed to Read-After-Write Compare to verify that sector has been correctly written.

READ-AFTER-WRITE COMPARE

1. Setup 'Scan Equal' command for 765.

2. Go to common Read/Write routine for execution using remaining 'Write Data' parameters.

3. During 'Scan Equal' execution, the 765 chip reads the specified sector data from the disk and compares it on a byte for byte basis with data in VDP RAM memory, except where >FF appears in either memory or on the disk. A data request is issued for each byte in memory and must be serviced by the CPU every 27 microseconds during the sector compare. Upon completion of the sector compare, the 765 sets its interrupt line which releases the CPU.

4. The CPU now reads the status and ID registers presented by the result phase of the 'Scan Equal' command. This resets the 765 interrupt. Any error conditions (scan not satisfied, no data, data overflow) cause up to 8 retries of 'Write Data' followed by 'Scan Equal'. An error which still exists after 8 retries is returned thru CPU RAM "STAT" location.

READ/WRITE SECTOR ('RDWR') - EXECUTES READING OR WRITING OF A SECTOR

1. Checks motor startup timeout (MOTSPD) and waits if motor is not up to speed.

2. Retriggers motor startup timer to monitor execution of FDC command.

3. Sends 9 byte Read or Write Data command to 765 FDC.

4. Enables Wait logic.

5. Calls Read or Write Byte Transfer loop now loaded in 16-bit fast RAM for execution of 256 byte data transfer.

6. Upon return from Byte Transfer loop, disables Wait logic and checks to see if motor startup timeout (850 msec. 1-shot) has expired. If timer is expired then 765 has locked-up in trying to read single density format while is double density mode. The FDC is reset and a retry is initiated thru the error handler routine which will switch density modes.

7. Any errors returned from the 765 FDC are processed thru the error handler, otherwise a normal return to the high level DSR is exercised.

RETURN TO HIGH LEVEL DSR ('RETURN')

1. Sets return status byte 'STAT' to zero if no errors

2. Restores saved contents of 16-bit CPU RAM.

3. Clears Saved Loop, Format, and Density Switched flags.

4. Turns off LED.

5. Returns to high level DSR.

FORMAT - WRITES SECTOR MARKS & ID'S ON DISKETTE
'FORMAT' or 'FORML'

1. Turns on board LED.

2. Calls 'SPECFY', 'RESTOR', and 'SAVLOP'.

3. Waits for motor to get up to speed.

4. Moves Write Byte Transfer Loop to 16-bit RAM.

5. Sets up VDP RAM buffer starting at "MEMSTA" for 765 format data.

6. Enables Wait logic.

7. Send 'Format a Track' command to 765 and specify bytes per sector, sectors per track, gap #3 length, and data pattern to be written into each sector data field. During execution, the 'Format a Track' command sends 4 data requests for each sector to obtain cylinder no., head no., sector number, and no. of bytes/sector to be written into the sector ID fields per IBM format. Sector numbers can be set up for interleaved sectors and for single density should be:
0,7,5,3,1,8,6,4,2 (9 sectors interleaved @4)
for double density:
0,2,4,6,8,A,C,E,1,3,5,7,9,B,D,F (16 sectors interleaved @8).
Upon completion of formatting a track, the 765 sets its interrupt which releases the CPU.

8. Disable Wait logic.

9. The CPU reads the returned 765 status registers. Any error condition, except write protected or locked-up FDC, causes up to 3 retries of 'Format a Track' before a hard error

10. If no error, send 'Seek' command to step head inward one track location. Then execute another 'Format a Track'. Continue until the number of cylinders per disk as specified in CPU RAM location "RW" >40 have been formatted

11. If 2 sides are specified ('SIDES'=2), Restore head and

Format Side 1.

12. Calculate the number of sectors/disk (Allocatable Units - AU's) and place in CPU RAM location "SEC" >4A. Place number of sectors/track in "RW" >4D.

7.0 PHYSICAL CHARACTERISTICS

7.1 WEIGHT

The total weight of an operational Double Density Disk Controller shall be less than 2 pounds.

7.2 SIZE

The Double Density Disk Controller shall have these nominal dimensions:

WIDTH: .9 inches
LENGTH: 7 inches
HEIGHT: 5 inches

7.3 STYLING

This product shall conform to the shape, color, and overall appearance of the approved styling model. all pictorial references to the product in owner's manuals, pretty boxes, point of purchase displays, and any other forms of advertising shall properly represent this styling model.

7.4 CASE

The Double Density Disk Controller case shall be made of injection molded plastics or die cast aluminum. The material used must be of sufficient durability to survive the anticipated environmental specifications to QRAS 10237, any pertinent governmental regulatory requirements and any other field use environment characteristic of the end use of the product.

7.5 INTEGRATED CIRCUITS

The main logic devices, microprocessors, memory devices, etc. shall meet the requirements of their individual component specification, and CPG 6.6 mos device specification. In addition, each IC must be qualified by either the vendor or CPG QRA in accordance with qras 10348.

7.6 DEVICE CONDITIONING

Specifics of the burn-in or pre-conditioning shall be called out in the individual piece part specification or purchase agreement. This specification merely defines the requirement.

7.7 POWER REQUIREMENTS

	MIN	MAX	
INPUT VOLTAGE	7.5	18	VOLTS
CURRENT	.5	.8	AMPS

7.8 EMI/RFI

Certification or verification, according to FCC rules, Part 15, Subpart J

7.9 ELECTRICAL SCHEMATIC

The electrical schematic is shown in TI drawing #1050302.

7.10 PARTS LIST

	QUANTITY	PART NUMBER	ITEM	EACH	TOTAL
	1	1500562-3016	74LS00 QUAD 2-NAND	.17	
	2	1500562-3017	74LS04 HEX INVERTER	.17	
	1	1501133-3008	74LS08 QUAD 2-AND	.18	
	1	1501260-3023	74LS11 TRIPLE 3-AND	.18	
	1	1500298-3001	74LS16 HEX INVERTER HVOC	.___	
	1	1500562-3019	74LS20 DUAL 4-NAND	.18	
	1	1501168-3008	74LS32 QUAD 2-OR	.18	
	2	1501260-3022	74LS38 QUAD 2-NAND OC	.18	
	2	1210095-3001	74LS74 DUAL FLIP-FLOP	.23	
	1	1501260-3009	74LS123 MULTIVIBRATOR	.45	
	1	1501620-3001	74LS125 QUAD TRI-BUFFER	.27	
	1	1501260-3012	74LS138 3-8 DATA SELECTOR	.33	
	1	1501621-3001	74LS153 DUAL 4-MULTIPLEXER	.31	
	1	1501260-3017	74LS156 DUAL 1-4 DECODER OC.	.40	
	1	1501638-3001	74LS161 SYNCH BIN-DIVIDER	.44	
	1	1500903-0001	74LS164 8 BIT SHIFT REG.	.42	
	3	1501260-0015	74LS244 OCTAL BUFFER	.69	
	1	1501260-3013	74LS245 OCTAL BUS TRANS.	.99	
	3	1501674-3001	74LS251 8-MULTIPLEXER	.31	
	2	1501682-3001	74LS259 8 BIT ADDR. LATCH	.62	
	1	1500442-0001	uPD765 FLOPPY DISK CONT.	12.50	
SPEC	1	_____-_____	FDC9216 DATA SEPARATOR	6.85	
ECN	1	1501392-_____	TMS4732 ROM	2.34	
ECN	1	1041016-_____	TMS4764 ROM	7.75	
	1	1501645-0001	MCM6810 RAM	1.20	
ECN	2	1500244-_____	HAL (PAL) 12L6	2.10	
	1	1500292-0001	7805C 5 VOLT REGULATOR	.40	
	1	1501643-0002	CRYSTAL 8 MHz	.63	
	1	1210081-0002	2N3904	.08	
	1	1039390-0019	LED YELLOW	.12	
SPEC	1	_____-_____	MINI-SWITCH 4 SPST	.___	
	1	1501063-0011	16 PIN LOW PROFILE SOCKET	.___	
	1	1039386-0001	60 PIN ATTLEBORO CONNECTOR	1.15	
	1	1039388-0001	34 PIN DIP .1" SPACE CONN.	1.89	
	1	1500773-0033	100 OHM	.___	
	16	1500773-0057	1k OHM	.___	
	2	1500773-0059	1.2k OHM	.___	
	1	1500773-0085	15k OHM	.___	
	1	1500773-0097	47k OHM	.___	
	2	1500773-0112	200k OHM	.___	
	1	1500499-0027	18 pF	.___	
	34	1501701-0098	.01uF	.___	
	1	_____-_____	4.7uF	.___	
	1	_____-_____	10 uF	.___	
	2	_____-_____	15uF	.___	
	2	_____-_____	47uF	.___	
	1	1050303	PRINTED CIRCUIT BOARD	.___	
		1050302	SCHEMATIC		
		1050320	PRODUCT SPECIFICATION		

7.11 ENVIRONMENTAL REQUIREMENTS

The Double Density Disk Controller shall meet all the requirements of this specification after exposure to the environmental requirements of TI QUAS 10237.

7.12 QUALIFICATION

The Double Density Disk Controller shall meet all the requirements of this specification and of TI QUAS 10237 at the conclusion of all testing requirements of TI QUAS 10237. This shall include, but not be limited to the following categories:

A) Mechanical stress testing (vibration, loose cargo), transportation tests, transportation handling, and customer handling.

B) Operation under temperature/humidity rapidly changing temperatures

C) Long term operation under anticipated/worst case conditions of temperature/humidity.

D) Long term storage under worst case temperature/humidity conditions.

E) Operating life tests to simulate field performance and predict return rate liability.

F) Electrical characterization for conformance to this specification, and any governmental regulatory or safety agencies such as UL, CSA, FCC, VDE, etc.

G) Resistance to static electricity.

H) Compatibility with peripheral products intended for use in conjunction with this product.

I) Any other category pertinent to this specific product.

7.13 QUALITY ASSURANCE PROVISIONS

All product production will be sampled per the applicable TI QUAS #_____ for conformance to the TI outgoing quality standards.

7.14 SUBCONTRACTED OR PURCHASED PRODUCT

All shipments of disk controllers received from non-TI facilities will be sample tested for conformance to this specification per QUAS 10308.